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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,948	08/03/2001	Michael Violette	303.017US4	1213

21186 7590 01/25/2005

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EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,948	VIOLETTE, MICHAEL	
	Examiner	Art Unit	
	Dana Farahani	2814	

-- The MAILING DATE of this communication appears on th cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-38 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-38 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 10-16, 25-33, 38, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Grubisich (US Patent 5,581,115), previously cited.

Regarding claim 10, Grubisich discloses in figure 2, a transistor formed in a semiconductor substrate ~~60~~ 40, the substrate having a first conductivity type and a surface, the transistor comprising:

a collector region, 44, having an impurity therein which promotes one of either holes or electrons as a majority carrier, the collector extending downward form the surface of the substrate, wherein the first conductivity type of the substrate promotes the other of either holes or electrons as a majority carrier;

a base region 52 having an impurity therein which promotes the other type of carrier, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector;

an emitter 50 on top of the base region and having a surface area, smaller than the surface area of the base region;

an implant region 58, in the collector region, an implant area of the collector region vertically adjacent to the base region having an increased collector doping of an implanted

impurity, the implant area having an effective surface area, which is in contact with the base region, greater than the surface area of the emitter and less than the surface area of the base region..

Regarding claims 11, 12, 14, 15, and 31, see Grubisich, column 12, lines 31-34, wherein it is stated that boron and phosphorus are used to make the p and n regions of the device, respectively (note that Grubisich discloses at column 16, lines 42-44 that a pnp transistor can be used as well).

Regarding claims 13 and 16, Grubisich discloses in figure 2, a transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region 44 having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region 52 having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region 50 on the base region, the emitter region having a surface area that is in contact with the base region and is smaller than a surface area of the base region;

and an implant region 58 interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective surface area greater than the surface area of the emitter region and less than the area of the base

region contiguous to the collector region, wherein the effective surface area is in contact with the base region.

Regarding claims 25 and 29, in figure 2, there is an emitter 50 having an emitter surface area;

a base 52 having a base surface area, wherein the emitter surface area is in contact with the base;

a collector 44 in contact with the base;

and an implant region 58 intermediate the base and the collector, the implant region having an implant surface area in contact with the base, the implant surface area being greater than the emitter surface area and less than the base surface area.

Regarding claims 26-28, the base surface area is less than that of the collector; the surface area of the implant region is less than that of the collector; and the base and implant region surface areas have a combined area greater than that of the emitter.

Regarding claim 38, in figure 2, there is an emitter 50 having a periphery and a lateral extent;

a base 52 having a lateral extent in contact with the emitter to define an emitter-base surface;

a collector 44 in contact with the base; and

means 58 for minimizing carrier injection from the periphery of the emitter region to the collector region at high current operation of the transistor, wherein the means includes a region in contact with the collector and the base, the region including a first surface in contact with the

base and a second surface in contact with the collector, the first surface having a larger lateral extent than the emitter-base surface and a smaller lateral extent than the base.

Regarding claim 30, an n well collector region (42 and 58) having an impurity of a first conductivity type, the collector region extending downwardly from a surface of the substrate 40, the substrate being generally doped with an impurity of a second conductivity type;

a base region 52 having an impurity of the second conductivity type doped at a generally constant doping level across a surface thereof, the base region extending downwardly from the surface of the substrate into contact with a portion of the collector region;

an emitter 50 having an impurity of the first conductivity type on top of the base region and having a surface area smaller than a surface area of the base region; and

an area 58 of the collector region vertically adjacent the base region having an increased collector doping of the first conductivity type, the area of the collector region having an effective surface area in contact with the base region that is greater than the surface area of the emitter.

Regarding claim 32, the effective surface area of the collector region is less than a non-increased doped area of the portion of the collector region in contact with the base region, as can be seen in figure 2.

Regarding claim 33, the transistor in figure 2 comprises a substrate 40, the substrate having a first conductivity type and a surface;

a collector region 42 having a first impurity means for promoting one of either holes or electrons as a majority carrier, the collector region extending downward from the surface of the substrate, wherein the first conductivity type of the substrate promotes the other of either holes or electrons as a majority carrier;

a base region 52 having a second impurity means for promoting the other type of carrier, the base region having a surface area and extending downward from the surface of the substrate into contact with a portion of the collector region;

an emitter region 50 on top of the base region and having a surface area smaller than the surface area of the base region; and

an area 58 of the collector region vertically adjacent to the base region having an increased collector doping of an implanted impurity, the implant area having an effective surface area that is in contact with the base region, greater than the surface area of the emitter region and less than the surface area of the base region, as can be seen in the figure.

Regarding claim 40, in figure 2 there is a transistor, comprising:

an emitter 50;

a base 52 in contact with the emitter to define an emitter-base surface;

a collector 42 in contact with the base to define a horizontal base-collector surface; and means 58 for minimizing base-collector capacitance and maximizing high current operation wherein the means includes a region in contact with the collector and the base, the region including a first surface in contact with the base and a second surface in contact with the collector, the first surface being larger than the emitter-base surface and smaller than the base-collector surface.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17-24 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grubisich.

Regarding claims 17 and 23, Grubisich discloses in figure 2, a transistor formed in a semiconductor substrate, the substrate including a surface and a region doped with an impurity which promotes one of either holes or electrons as a first majority carrier, the transistor comprising:

a collector region 42 having an impurity therein which promotes the other of holes or electrons as a second majority carrier, the collector region extending from the surface of the substrate;

a base region 52 having an impurity therein which promotes the first majority carrier, the base region extending from the surface of the substrate into contact with a portion of the collector region;

an emitter region 50 on the base region, the emitter region having a surface area smaller than a surface area of the base region;

a first implant region 58 interposed between the collector region and the base region, the implant region having an increased doping of an implant impurity and having an effective surface area greater than the surface area of the emitter region contiguous to the base region and less than the area of the base region contiguous to the collector region.

Grubisich does not disclose a second implant region formed in the collector region.

Grubisich discloses in figure 5a, an implant region 90 in the BJT device shown in that figure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a second implant area in the collector region in order to make a collector contact.

Regarding claim 18, the second implant region would be formed at about the same level from the surface of the substrate as the first implant.

Regarding claims 19, 20, and 34-37, Grubisich discloses the limitations in these claims, as discussed above with respect to claim 17. Also, note that the implant region 90 is formed in the plug region, that is the region that directly surrounds region 90. Also, a sub-region of region 90 at the same depth of the implant region 58 forms the second implant in region 90.

Regarding claims 21 and 22, see Grubisich, column 12, lines 31-34, wherein it is stated that boron and phosphorus are used to make the p and n regions of the device, respectively (note that Grubisich discloses at column 16, lines 42-44 that a pnp transistor can be used as well).

Regarding claim 24, the second implant (the middle portion of plug 90) in figure 5a has a surface area greater that the surface area of the opening at the top of it.

Product-by-Process Limitations

In claims 36 and 37, the implant regions "being simultaneously formed by an angled implant", or "by the same source" are considered methods of forming those regions and not limitations of the final product. Therefore, such limitations are given no patentable weight.

The Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao,* 190

USPQ 15 at 17 (footnote 3). See also, *In re Brown,* 173 USPQ 685; *In re Luck,* 177 USPQ 523; *In re Fessmann,* 180 USPQ 324; *In re Avery,* 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe,* 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Response to Arguments

5. Applicant's arguments with respect to the rejected claim have been considered but are moot in view of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

1/21/05